**Amendments to the Drawings:**

Figures 7A and 7B are amended to correct the size of memory module 80D to be 512 MB instead of 521 MB. This amendment is supported in paragraph 0037 of the specification, and no new matter is added. Acceptance of the corrected figures is respectfully requested.

Attachment: Replacement Sheets 2 pages

## REMARKS/ARGUMENTS

1. Objections to the specification and claims.

**Response:**

Paragraphs 0007, 0024, 0025, and 0035, along with the abstract have all been amended to correct informalities. The applicant has corrected all errors that were found by rereading the specification.

Claims 1-13 are cancelled, and are no longer in need of consideration.

Claim 17 has been amended to correct informalities.

Claim 18 has been amended to change "XOR" to "NXOR", and is now consistent with both the specification and the drawings. Acceptance of the corrected specification and claims is respectfully requested.

2. Claims 1, 8, and 18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

**Response:**

Claims 1 and 8 have been cancelled, and are no longer in need of consideration. Claim 18 has been amended to change "XOR" to "NXOR", and is now consistent with both the specification and the drawings. Reconsideration of claim 18 is respectfully requested.

3. Claims 1-13 are rejected under 35 U.S.C. 101 because the claimed inventions are directed to non-statutory subject matter.

**Response:**

Claims 1-13 are cancelled, and are no longer in need of consideration.

4. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koos (US 4,400,794) in view of Schmisseur et al (US 6,128,718) and Hirschberg ("Data Compression").

**Response:**

Claims 1-13 are cancelled, and are no longer in need of consideration. Claim 14 contains the limitation of "a sorting module for making the corresponding address of the section with greater size smaller than the corresponding address of the section with smaller size, and if the size of a first section is equal to the size of a second section, the first and the second sections are capable of being swapped". On the other hand, Hirschberg discloses constructing the codes according to probabilities, and does not disclose assigning the address according to the memory size. Therefore, the cited prior art does not teach this limitation of claim 14. Furthermore, Schmisseur et al. does not teach the "bit-pattern" as it is described in the instant application, and also does not teach that the given address is compared with the bit-pattern, as is recited in independent claim 14. Therefore, claim 14 is patentably distinguished from the cited prior art. Claims 15-17 are dependent on claim 14, and should be allowed if claim 14 is allowed. Reconsideration of claims 14-17 is respectfully requested.

5. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koos in view of Schmisseur et al Hirschberg, and further in view of Handy ("Binary Operations").

**Response:**

As to claim 18, the combination of Koos, Schmisseur et al, and Hirschberg fails to

teach the plurality of NXOR gates and the second level AND gate. Although Handy ("The Cache Memory Book") teaches a plurality of XOR gates and a second level AND gate, Handy does not teach the comparing module having a plurality of NXOR gates connected to a second level AND gate as is claimed. Therefore, the currently amended claim 18 should be patentable over the cited prior art.

6. Claims 1-4, 8-11, and 14-17 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-2, 4-5, 12-14, and 16 of copending application number 10/708,103 in view of Hirschberg.

**Response:**

Independent claim 12 of the copending application number 10/708,103 has been amended to considerably narrow the scope of this claim. As such, the claims of the instant application are no longer unpatentable over copending application number 10/708,103 in view of Hirschberg.

7. Introduction to new claims 19-33:

New independent claims 19 and 33 have been drafted based on the original claim 1. Claims 19 and 33 recite "obtaining at least one bit-pattern of each section according to the common rules of the bit of the addresses" and "comparing the given address with each bit-pattern to determine the objective section of the given address". Claims 19-33 are supported by the original claims 1-18, and no new matter is added.

Koos does not disclose using the bit-pattern, obtained according to common rule of bits, for each section of memory, and comparing if bits of the given address match those in the bit-patterns. In addition, Schmisseur et al also does not teach the claimed bit-pattern of the addresses, and comparing the given address with each bit-pattern. Therefore, the cited prior art fails to teach "comparing the given address with each bit-pattern to

determine the objective section of the given address" as is claimed. Acceptance of the new claims 19-33 is respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu Date: June 29, 2006

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)